4-2 COMPRESSOR

ABSTRACT OF THE DISCLOSURE

A compressor of a multiplier according to an embodiment of the present invention includes a first compressor, in which the first compressor includes a first plurality of inputs. The first compressor also includes a summation output, a first carry bit output; and a first plurality of transistor paths connecting each of the first plurality of inputs to the summation output. The compressor also includes a successive compressor, in which the successive compressor includes a second plurality of inputs and a plurality of successive transistor paths connecting at least one of the first plurality of inputs to the first carry bit output and connecting the first carry bit output to at least one of the second plurality of inputs. In one embodiment of the present invention, a first compressor critical transistor stage path level within the first compressor is less than seven and a successive compressor critical transistor stage path level within the successive compressor is less than eight. In another embodiment of the present invention, a first compressor critical transistor stage path level within the first compressor is less than eight and a successive compressor critical transistor stage path level within the successive compressor is less than seven.